IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application		)	PATENT APPLICATION	
Inventors:	Adrian J. Isles	)	Art Unit:	2123
Application No.:	09/586,191	)	Examiner:	Sharon, Ayal I.
Filed:	June 2, 2000	)	Customer No.	28554
Title:	CIRCUIT-LEVEL MEMORY AND COMBINATIONAL BLOCK MODELING	)		

DECLARATION OF ADRIAN J. ISLES UNDER 37 C.F.R. §1.132

I, Adrian J. Isles, hereby declare:

1. I am the inventor of the invention claimed in United States Patent Application Ser. No. 09/586,191 ("the present application").

2. I received a Bachelor of Science in Electrical Engineering from Howard University in 1993, a Masters of Science in Electrical Engineering and Computer Science from the University of California at Berkeley in 1997, and Ph.D in Electrical Engineering and Computer Science from the University of California at Berkeley in 2000.

3. In 1999, I began working at Averant as a Member of the Research and Development Consulting Staff, where my responsibilities included development of formal verification algorithms. In 2003, I became "Principal Architect" at Averant, Inc. which is my current position. My responsibilities include architecture development for simulation and verification software as well as developing formal verification algorithms for complex integrated circuits.

4. Averant, Inc., the assignee of the present application, is a leader in verification software tools for electronic circuit designs. The Company's Solidify tool provides an interactive, easy-to-use design tool for static functional verification. Design quality can be improved, design cycles shortened, and unnecessary simulation eliminated with Solidify. Besides RTL verification, Solidify detects inconsistencies coming from functional specifications, and includes code coverage technology for verification assurance. In one tool, Solidify, offers

designers a better alternative to test vector generation, functional simulation, and code coverage by using a static approach without vectors.

5. I have read the present application and am familiar with the claims currently pending after entry of the reply entitled Response B to Office Action under 37 C.F.R. § 1.111. I have also read and analyzed the Office Actions and the prior art used in the rejections set forth in the Office Actions.

6. My comments in this Declaration pertain to factual matters as understood by one of ordinary skill in the art. These factual matters pertain to the scope and content of the prior art, the level of ordinary skill in the pertinent art, and the differences between the prior art and the claims at issue.

7. In regard to the present application, it is my belief that the level of ordinary skill in the art pertains to a person with an undergraduate degree in Computer Science (or equivalent), 2-4 years experience in software simulation and verification tools, and an understanding of how to program such tools. I made this determination based on my own experience prior to conceiving of the invention of the present application. The information set forth below as the Background of the Technology at Issue provides a description of the relevant technology as understood by one of ordinary skill in the art.

A. Background of Technology at Issue

8. The subject matter of the present application relates to electronic design automated (EDA) systems and memory models that can be used with such design systems. The design process for integrated circuits typically involves multiple transformations of a design from an initial idea to a functional, manufacturable product. A chip architect or designer begins with a design idea and then generates a corresponding behavioral definition of the design. The behavioral design results in a flow chart or a flow graph using which the designer can design the system data path and the registers and logic units necessary for implementation of the design. After the designer designs buses for coordinating and controlling the movement of data between registers and logic units, the data registers, buses, logic units, and their controlling hardware are implemented using logic gates and flip-flops. The result of this design stage is a netlist of gates and flip-flops. The netlist can be used to create a simulation model of the design to verify the design before it is built. Once the design has been verified, the netlist can be used to provide the information needed by a routing software package to complete the actual design. The netlist of

gates and flip-flops is thus transformed into a transistor list or layout and gates and flip-flops are replaced with their transistor equivalents or library cells. Timing and loading issues are also addressed during this cell and transistor selection process. Finally, the manufacturing process begins when the transistor list is implemented in a programmable logic device such as an FPGA or when the layout specification is used to generate masks for integrated circuit fabrication.

9. EDA tools improve upon this design process by permitting electronic circuit designers to more quickly and inexpensively design and verify their designs. A typical design approach using EDA tools can begin by a designer initially supplying a logic synthesis tool with a high level language description of the design and the logic synthesis tool reducing the high level language description to a low level or gate level description of the design. Finally, verification or simulation of the design is performed by an engine using a set of properties or behaviors as an input to determine whether, and to what extent, the design described by HDL description satisfies the properties. The properties are based on a functional specification for the design being verified or simulated.

10. Such a design approach has been used to model, synthesize, and verify memory circuit designs. However, such prior art memory models suffer from two major disadvantages. First, some prior art memory models model every location of the memory even if only a subset of locations of the memory were needed to perform verification. For example, consider the case of a electronic design description that contains a RAM with 1024 memory locations along with one read port and one write port. If on each cycle, one memory read operation and one memory write operation can occur simultaneously and the designer would like to model the behavior of the RAM over five clock cycles, then only 10 locations (2 memory locations per clock cycle * 5 clock cycles) need to be modeled, not 1024, as required by such prior art memory models. Verifying or simulating a memory model that contains all 1024 locations is inefficient and wastes valuable resources. Second, memory models from one EDA tools vendor can typically only be used with simulation or verification engines from the same vendor. In other words, the choice to use a particular prior art memory model necessitates a particular verification or simulation engine in these approaches. This lack of interoperability greatly limits the utility of prior art memory models.

B. The Combination of *Weems* and *Murgai*

11. Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching, 1996 ("*Weems*") is directed to cache memory which is a physical "small and fast memory" used in computing systems. *Weems*, p. 2. Cache memory is an actual physical structure used to store data. As taught by *Weems*, values in the subset of main memory that are being accessed repeatedly are copied "from slower memory to the small fast memory [cache]" which can consist "of lines of data, usually containing data from two or more consecutive addresses of main memory." *Id.* at pp. 2-3. 12. *Weems* is concerned with designing memory systems for computers that will maximize the performance (in terms of the speed of performing memory read and write operations) of the physical implementation of the computer memory while minimizing the cost of manufacturing the physical implementation of the computer memory. *Weems* achieves this goal by way of using memory hierarchies. Such hierarchies include cache memories, which are small, fast and relatively expensive memories systems that act as an intermediaries between the computer's main processor and the large, slow and relatively inexpensive main memories (such as RAMs) which are found in modern computer systems. *See Weems*, pp. 2-7. Weems discusses techniques for copying data form the slower, larger, memories to the smaller, faster cache memories (and vise-versa). *Id.* He also shows how such systems and related techniques can be implemented using look up tables and other structures. *Id.* at ppl. 10-11. Absolutely nowhere in *Weems* does the author discuss approaches of how electronic design descriptions that contain memories (such as RAMs) can be modeled (by using lookup tables or any other method) for efficient simulation and verification using an EDA tool.

13. Murgai, R. et al., *Logic Synthesis for Programmable Gate Arrays*, 27th ACM/IEEE Design Automation Conference, 1990 ("*Murgai*") is directed to synthesizing "'high-level description' (like equations or a VHDL description) of a circuit" onto programmable gate array architectures. *Murgai*, 1. Introduction. *Murgai* is not concerned with memory or memory models at all but rather the synthesis of descriptions onto physical programmable device structures. *Murgai* directs his teachings to the physical implementation of circuit descriptions onto physical structures, namely programmable gate array architectures. Absolutely no where does Murgai discuss approaches of how electronic design descriptions that contain memories (such as RAMs) can be modeled (by using lookup tables or any other method) for efficient verification using an EDA tool.

14. One of ordinary skill in the art, presented with both the *Weems* reference and *Murgai* reference would not be motivated or suggested to somehow combine cache memory techniques with logic synthesis techniques for programmable gate arrays. From the perspective of one of ordinary skill in the field of electrical engineering and computer science, the teachings of *Weems* and *Murgai*

are disparate and related only in the very loose sense that they concern some phase of the design, development, and physical implementation of electronic systems. *Weems* is in the area of Computer Architecture. There is nothing in *Weems* that would suggest taking such a data storage technique and combining it with techniques for realizing a physical implementation of a circuit description using a programmable gate array. *Weems* repeatedly grounds his teachings in a central processing unit context and provides no suggestion for expanding the memory techniques therein to synthesizing circuit level descriptions. Likewise, *Murgai* is directed to synthesizing circuit level descriptions onto PGA's. There is nothing in *Murgai* to suggest the expansion of the described techniques into a computing environment where cache memory is used to increase performance in data retrieval. Programmable gate arrays are a type of device that can be programmed to implement a logic function and it is not clear how this would be combined with cache memory techniques in a computing environment to achieve a desired result taught by either reference.

15. Neither *Weems* nor *Murgai* is in the same field of endeavor as Applicant's claimed invention. Applicant's claimed invention is directed to creating an abstract model of a physical memory using a lookup table and using the lookup table in a description of an electronic circuit that can be used primarily for the propose of verifying (or simulating) the design containing the memory. *Weems*, however, is directed to cache memory techniques in a computing environment and *Murgai* is directed to taking a circuit level description and realizing a functional physical device. These teachings are not in the field of modeling physical memories in circuit level descriptions. *Weems* is directed to the temporary storage of data in a computer while *Murgai* is directed to taking an already developed description and synthesizing it onto a physical architecture. There is nothing the relevant field of art of the claimed invention to suggest combining such references in distinct fields of endeavor.

C. <u>The Combination of *Bayoumi* and *Murgai*</u>

16. Bayoumi, M. et al., *A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications*, IEEE Transactions on Circuits and Systems, Vol. 34, Issue 6, June 1997, pp. 604-616 ("*Bayoumi*") is directed to the field of art typically referred to as integrated circuit (IC) design. *Bayoumi's* teachings are directed to methodologies for creating integrated circuits for digital signal processing architectures that use a special form of arithmetic called the Residue Number System (RNS). *Bayoumi*, p. 604. *Bayoumi* discusses how RN systems have been shown to be suitable for the physical implementation using networks of look-up tables which are interconnected together on an integrated circuit. *See id.* at pp. 604, 606-607, 610-611. In particular, the disclosure is concerned with the methodology of choosing the size of each lookup table in terms of the number of

bits involved, area, width, timing, delay, etc. of the physical implementation. *See id.* at pp. 607-610. While the terminology in *Bayoumi* is somewhat confusing, one of ordinary skill in the art would understand the term "memory module" to which *Bayoumi* refers to refer to as a storage array and supporting circuitry necessary to physically implement a lookup table on an integrated circuit. *See id.*. at pp. 606-607. One of ordinary skill in the art would understand the term "memory model" to refer to a mathematical tool employed to help determine the best way (in terms of area and access time) to implement the lookup table on an integrated circuit. *See id.* at pp. 607-608.

17. *Bayoumi* does not address methods for how to model memory read and write operations or uninterpreted combinational blocks, nor would one of ordinary skill in the art understand such methods to be relevant to the disclosure in *Bayoumi*. *Bayoumi* is directed to a model that simulates the physical layout of a memory module such as a lookup table that represents the basic building block unit of the RNS memory intensive architectures. In *Bayoumi*, the lookup table is the actual physical memory to be laid out on a chip, not a model of a physical memory. Absolutely nowhere does *Bayoumi* discuss approaches of how electronic design descriptions that contain memories (such as RAM) can be modeled (by using lookup tables or any other method) for efficient verification using an EDA tool.

18. One of ordinary skill in the art, presented with both the *Bayoumi* reference and *Murgai* reference, would not be motivated or suggested to somehow combine the teachings directed to physical networks of lookup tables which are interconnected on an integrated circuit with teachings directed to the synthesis of high-level descriptions onto lookup table architectures. From the perspective of one of ordinary skill in the field of electrical engineering and computer science, the teachings of *Murgai* and *Bayoumi* are disparate and related only in the very loose sense that they concern some phase of the design, development, and physical implementation of electronic systems. Neither reference contains any disclosure relevant to models of physical memories. Each reference is in someway directed to the actual physical memory itself, either by way of a network of interconnected physical lookup tables or the synthesis of designs onto physical lookup tables. Nothing within either reference or the knowledge of those of ordinary skill in the art suggests anything relating to lookup tables which are models of physical memory used in electronic circuit design descriptions.

D. Claims 1-11, 29-33, 45-47, and 51

19. The method recited in claim 1 models memory read and write operations of an electronic circuit design using a lookup table. A portion of a description of the electronic circuit design is then replaced with the lookup table such that the lookup table in the description represents the physical memory.

20. One of ordinary skill in the art would understand Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching, 1996 ("*Weems*") to disclose caching techniques for temporarily storing data in smaller and faster memory to increase data access performance in computer systems. As *Weems* teaches, a "cache consists of lines of data, usually containing values from two or more consecutive addresses of main memory." *Weems*, p. 3. One of ordinary skill in the art would understand a cache memory as disclosed by *Weems* to be a physical memory structure that physically stores data. One of ordinary skill in the art would further understand *Weems* to disclose a lookup table that is used for mapping from a virtual address space to a physical address space. As *Weems* teaches, in "order to perform the mapping function, a table lookup is employed." *Id.* at p. 11.

21. One of ordinary skill in the art would not understand the cache memory and techniques disclosed by *Weems* as modeling memory read or write operations of an electronic circuit design in a lookup table. Rather *Weems* teaches that a cache memory, which can be physically implemented using lookup tables; can be used to speed up the read or write operations of a physical memory structure and that lookup tables can also be used for the purpose of mapping a virtual address space to a physical address space. *See Weems*, pp. 2-8, 10-11. *Weems* teaches that a read operation of a cache involves a comparison of the address from a memory reference against the tags stored in cache. "If there is a match, then the line of data is read from the cache and the low order bits of the address select the appropriate word from the line to be passed to the CPU." *Id.* at p. 3. For write operations, *Weems* teaches that "we can write it [value] to the cache and simultaneously write it in through to the main memory so that the master copy is kept up to date. Or, we can write it to the cache and not write it back to the main memory until it is replaced." *Id.* at p. 7. Weems contains no disclosure relating to modeling memory operations for electronic circuit designs. For example, Weems does not present any method for modeling a physical memory such that the verification of an electronic circuit design description that contains such a memory can be done efficiently. Read and write operations involving cache memory as described by *Weems* do not relate to modeling memory operations of

electronic circuit designs. *Weems* addresses physical memory and related data storage techniques in computing environments. As such, *Weems* does not teach the steps of "modeling a memory write operation of the electronic circuit design using a lookup table," and "modeling a memory read operation of the electronic circuit design using a lookup table."

22. One of ordinary skill in the art would understand Murgai, R. et al., *Logic Synthesis for Programmable Gate Arrays*, 27th ACM/IEEE Design Automation Conference, 1990 ("*Murgai*") to disclose logic synthesis techniques for programmable gate arrays (PGA). One of ordinary skill in the art would understand that PGA architectures consist of repeated arrays of logic blocks which are also called basic blocks. One category of block structures is Table Look-Up. One of ordinary skill in the art would understand a Table Look-Up block structure to be a physical structure. One of ordinary skill in the art would understand *Murgai* to disclose techniques for synthesizing high-level descriptions onto Table Look-Up architectures.

23. The Examiner has asserted that *Murgai* teaches that "equations or VHDL are used to 'model' the Table Look-Ups used in programmable gate arrays (PGA)." *Office Action dated February 25, 2004*, p. 6. One of ordinary skill in the art would not understand *Murgai* to teach the use of equations or VHDL to model a Table Look-Up architecture as asserted. A Table Look-Up architecture is a predefined physical block structure onto which a high-level description is synthesized. For example, *Murgai* teaches "tak[ing] a 'high-level description' (like equations or a VHDL description) of a circuit and sythesiz[ing] onto these architectures." *Murgai*, p. 620, Introduction. *Murgai* does not disclose a high-level description that models a Table Look-Up architecture of a PGA but rather the synthesis of a description onto one of these architectures. The teaching of synthesis of high-level descriptions onto PGA architectures including Table Look-Up is not a teaching of equations of VHDL used to model the Table Look-Ups, as the Examiner asserts. Furthermore, claim 1 recites "modeling a memory write [read] operation of the electronic circuit design using a look-up table." In claim 1, the look-up table is the model, not what is modeled as the Examiner asserts. As such, *Murgai* does not teach the step of "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and wherein the lookup table in the description represents the physical memory."

E. <u>Claims 12-13, 42-44, 48</u>

24. The invention recited in claim 12 utilizes a lookup table to model an uninterpreted

combinational block of an electronic circuit design. An uninterpreted combinational block is a part of an electronic design description in which the inputs and outputs of the block are given, but whose actual functionality remains undefined. The lookup table is used in a description of the electronic circuit design to represent the uninterpreted combinational block of the electronic design.

25. *Weems* teaches cache memory techniques in computer systems. *Weems* does not contain any disclosure relating to descriptions of electronic circuit designs or models used in descriptions of electronic circuit designs. *Weems* does not contain any teachings of lookup tables that model uninterpreted combinational blocks of electronic circuit designs. As such, *Weems* does not teach "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combination block, and wherein the lookup table in the description represents the uninterpreted combinational block."

26. *Murgai* does not contain any disclosure relating to lookup tables that model uninterpreted combinational blocks of electronic circuit designs. *Murgai* teaches techniques for synthesis of high-level descriptions onto PGA Table Look-Up block structures. One of ordinary skill in the art would understand the Table Look-Up structure to be a physical structure on which designs are realized. Thus, *Murgai* does not disclose "replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combination block, and wherein the lookup table in the description represents the uninterpreted combinational block."

F. Claims 14-22, 34-40, and 49

27. The invention recited in claim 14 utilizes a memory model to represent physical memory in a description of an electronic circuit design. A portion of a description of the electronic circuit relating to the physical memory is replaced with the memory model.

28. *Weems* does not contain any disclosure relating to descriptions of electronic circuit designs or models used in descriptions of electronic circuit designs. As such, *Weems* does not teach "modeling a memory write operation of the electronic circuit design in a memory model to represent a memory write operation in the physical memory," or "replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the electronic circuit design relates to the physical memory, and wherein the memory model in the description represents the physical memory."

29. *Murgai* teaches techniques for synthesis of high-level descriptions onto PGA Table Look-Up block structures. The Table Look-Up block structures are physical block structures, not models of memory. *Murgai* does not contain any disclosure relating to memory models that represent memory write operations in physical memory. Thus, *Murgai* does not teach "modeling a memory write operation of the electronic circuit design in a memory model to represent a memory write operation in the physical memory," or "replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the electronic circuit design relates to the physical memory, and wherein the memory model in the description represents the physical memory."

G. <u>Claims 23-28 and 50</u>

30. Claim 23 recites a method using lookup tables that includes various steps in the electronic design synthesis and verification. A hardware description language description of the lookup table is created that represents physical memory of the circuit design. The description language is synthesized to a gate level description and then verification of the design is performed.

31. One of ordinary skill in the art would understand Bayoumi, M. et al., *A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications*, IEEE Transactions on Circuits and Systems, Vol. 34, Issue 6, June 1997, pp. 604-616 ("*Bayoumi*") to disclose design methodologies based on the realization of a model for the layout of a set of lookup tables that are interconnected together. *Bayoumi*, p. 607. The design methodologies develop a look-up table layout model and select efficient layouts according to design requirements by allowing the designer to control the area, time, or the configuration of the lookup table required for implementing certain types of digital signal processing architectures. *See id.* at pp. 607-610. These modules are based on having several look-up tables connected together in the same package. One of ordinary skill in the art would understand these modules for implementing look-up tables to be physical devices laid out in the VLSI design.

32. One of ordinary skill in the art would not understand *Bayoumi* to disclose lookup tables used in hardware description language descriptions of electronic circuit designs. The lookup tables of *Bayoumi* are physical structures. *Bayoumi* teaches that the "modules are based on having several look-up tables connected together in the same package." *Bayoumi*, p. 607. Thus, the look-up tables of *Bayoumi* are the actual physical devices to be laid out. They do not

model memory operations of a memory in circuit descriptions. Actual physical look-up tables as disclosed by *Bayoumi* are not the same as a lookup table or hardware description language that "represents the physical memory of the electronic circuit design," as recited in claim 23. They are actual physical structures to be placed or implemented in an actual circuit. As such, *Bayoumi* does not disclose "creating a hardware description language description of the lookup table and a plurality of components of the electronic circuit design, wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design."

33. *Murgai* teaches techniques for synthesis of high-level descriptions onto PGA Table Look-Up block structures. One of ordinary skill in the art would understand the Table Look-Up structure to be a physical structure on which designs are realized. As such, *Murgai* does not teach creating hardware description languages of lookup tables. *Murgai* teaches the synthesis of descriptions onto these Table Look-Up structures. Thus, *Murgai* does not disclose "creating a hardware description language description of the lookup table and a plurality of components of the electronic circuit design, wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Executed in Alameda, California on August 25, 2004.

Adrian J. Isles